

Amendments to the Specification

Please replace the paragraph on page 1 beginning on line 25 with the following amended paragraph:

As shown in Figure 1, in accordance with LSSD rules, shift register latches (SRL's) 100 on a semiconductor chip 102 are joined together to form a shift register LSSD scan latch chain 104 to facilitate testing of combinational logic blocks 106, 108 and 110 interconnected by the SRLs 100 of the scan latch chain 104. Data is inputted to the combinational logic blocks 106, 108 and 110 and the SRLs 100 in a parallel respective primary inputs (PIs) 112 of the chip 102. Data is outputted from the combinational logic blocks 106, 108 and 110 and the SRLs 100 in parallel through the primary outputs (POs) vectors 114 of the chip 102. During testing, the scan chain latch circuits [[104]] 100 may also be loaded serially. Serial input (SRI) 116 provides a serial input to the scan chain latch circuits 104. Similarly, serial output (SRO) 118 provides an output from scan chain latch circuits 104. Scanning inputs into the serial input SR 116 and out serial output 118 enables testing the SRLs 104 independently of the combinational logic 106, 108 and 110. It also allows each of the individual SRLs to be used as a pseudo-primary input or a pseudo-primary output for a combinational logic block 106, 108 or 110. The logic circuits in each of the logic blocks to be tested separately of circuits in other of the logic blocks.

Please replace the paragraph on page 4 beginning on line 18 with the following amended paragraph:

Figure 2 shows a typical configuration for a LBIST circuit 200, shown in U.S. Patent #5,983,380, the contents of which patent is hereby incorporated by reference. In that LBIST circuit, SRLs in the SRL chain 202 (with serial inputs (SIs) and serial output (SRO)) perform both input data launching and output data capturing. The test patterns come from a scan path that is configured into a linear feedback shift register (LFSR) 204. The test data are then outputted into the multiple input shift register (MISR) 206 for data compression. Alternate scan path shift cycles are applied to the SRLs exercising the combinational logic with the contents of the SRLs and capturing the results of the response of the combinational logic back into the SRLs where they are used as the test inputs for the next cycle. At the end of the requisite number of cycles, the contents of the scan path is read out as the signature to be compared with the desired value. As pointed out previously, a major drawback of LSSD test methodology is encountered when a LSSD scan chain circuit is not functioning properly and access to the internal logic of the circuit is greatly reduced. This is often the case early in a product's introduction cycle when the yields are relatively low or even zero. In these situations, the rapid determination of the fault's root cause is critical but not easily diagnosed. A primary cause of LSSD scan chain malfunctioning is when there is a stuck-at 0 or 1 fault stage 210 in a SRL scan chain 202.

Please replace the paragraph on page 5 beginning on line 13 with the following amended paragraph:

SRL scan chain 320 in Figure 3 is a type of the scan chain circuits found in Figures 1 and 2. It comprises a plurality of shift register latches (SRLs) 300 (herein designated as SRL₁, SRL₂, ..., SRL_{N-1}, SRL_N) in which each SRL 300 includes a master latch 308 and a slave latch 310. For transfer of data between the latches and combinational logic, 106, 108 and 110 such as that shown in Figure 1, each of the SRLs 300 contains a data input terminal 302 from combinatorial logic circuits and a data output terminal 304 to combinatorial logic circuits. In addition, data can be introduced into the latches at shift register input (SRI) terminal 316 and transferred from one SRL to another to the shift register output (SRO) terminal 318. As described below, data is clocked into each SRL 300 by applying a clock pulse to master latch 308, and data is clocked out of each SRL 300 by applying a clock pulse to slave latch 310. Data is outputted from slave latch 310 to a succeeding master latch 308. For this purpose, the operation of the LSSD scan chain 320 is controlled by scan clock signals on the a-clk, b-clk and c-clk lines. Serial loading of the master latch 308a from the [[SRL]] SRI 316 occurs upon generation of an a-clk pulse on a-clk line. The a-clk pulse on a-clk line causes serial input applied to the SRLs 300 to be inputted to each master latch 308. Application of a b-clk on b-clk line causes data to be output from the SRLs via slave latches 310. The continuous, alternating application of a-clk and b-clk clock pulse signals on the a-clk and b-clk lines respectively, sequentially propagates a data signal applied to SRI terminal 316 through scan chain 320 to SRO terminal 318. To effect a parallel load, a c₁-clk block pulse is applied to c₁-clk line. This causes a parallel load of data via parallel data inputs 302 and combinational logic to each master latch 308 of the SRLs 300.

Application of a b-clk or c₂-clk pulse to the b-clk line causes a parallel output of data from each slave latch 310 of SRLs 300 to provide data on respective parallel output data lines 304.

Please replace the paragraph on page 6 beginning on line 6 with the following amended paragraph:

As shown in Figure 4, with one of the SRLs 400 in the scan chain 320 stuck-at fault, the output 404 at the SRO of the LSSD scan chain 320 will [[be]] change to a string of all “0s” or “1s”. As shown, the change in data in the string is to all “0s” which is either after data (101010) from the latches 406 to [[412]] 410 succeeding the bad latch 400 are shifted out the stuck-at fault state of the failing latch 400 or the ~~invert of that state~~. Since the stuck-at fault latch 400 is intermediate, the input SRI and the output SRO of the chain 320, it is impossible to pass data down the LSSD chain 320 to determine the exact position on the failing bit 400 in the LSSD chain 320. In accordance with the present invention, disturb sequences are applied to the LSSD chain to cause one or more latches in the chain after the stuck-at fault latch 400 to change state from that transmitted to it by the stuck-at fault [[patch]] latch 400, and then the LSSD chain is run to pass the states of the various latches to its output SRO. By counting back from the output signal 408 produced by the last bit 410 in the chain 320 to the output signal 412 furthermost from the output signal 408 to have changed state, the location of the latch 406 producing the change can be determined . The assumption is that after running all disturb sequences of the test the changed data bit 412 is from the latch 406 adjacent to the failing latch 400 and that all the latches 406 to 410 are good.

Please replace the paragraph on page 6 beginning on line 25 with the following amended paragraph:

As shown at 600 in Figure 6, ~~during~~ the expected value for all the latches in the scan chain is set to the output's stuck-at level (i.e. Exp"0" for the stuck-at-0 chain or Exp"1" for the stuck-at-1 chain). This expect value is compared at 602 with the actual output from the scan chain for failure of any bit position to be in its expected value.

Please replace the paragraph on page 7 beginning on line 3 with the following amended paragraph:

If either initially or after any disturb step 500 such a failure is detected at [[606]] 604, the latch furthest from the scan chain output to fail is determined 606 and all expects for latches following and including that farthest failing latch are masked out (Exp"x") 608 so that they are no longer considered.